L Number	.2:43 .2:45 .2:44 .2:45 .2:45
3 9 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 (insert\$3 or add\$3) same (shift near4 register) and cyclical\$3 with address\$3 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory and @ad<20000920 10 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory and @ad<20000920 11 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3 and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3 and (shift near4 register) and cyclical\$3 with address\$3 with memory and @ad<20000920 10 40 (insert\$3 or add\$3) same delay\$3 and (shift near4 register) and cyclical\$3 with address\$3 with memory and @ad<20000920 (shift near4 register) and cyclical\$3 with address\$3 with address\$3 with memory and @ad<20000920 (shift near4 register) and cyclical\$3 with address\$3 with address\$3 with address\$3 with memory and @ad<200000920 (shift near4 register) and	.2:43 .2:45 .2:44 .2:45 .2:45
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memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or b	.2:45 .2:45 .2:45 .2:46
Tegister same cyclical\$3 with address\$3	.2:44 .2:45 .2:45 .2:46
56	.2:44 .2:45 .2:45 .2:46
register) and cyclical\$3 with address\$3 (insert\$3 or add\$3) same delay\$3 and register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3) and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and 41 (shift near4 register) and cyclical	.2:45 .2:45 .2:46
10	.2:45 .2:45 .2:46
(memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 9	.2:45 .2:45 .2:46
register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and &d<20000920 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3) and &d<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and &d<20000920 16 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory	.2:45 .2:46
With memory	.2:45 .2:46
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register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3) and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory and @ad<20000920	.2:46
with memory) and @ad<20000920 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) and cyclical\$3 with address\$3) and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory 12 5 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 16 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and (shift near4 register) and cyclical\$3 with address\$3 with memory with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory with memory) and @ad<20000920	.2:46
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and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory and @ad<20000920	.2:47
11 5 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 16 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and with memory ((insert\$3 or add\$3) same delay\$3 and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920	.2:47
(memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 (insert\$3 or add\$3) same delay\$3 and with memory ((insert\$3 or add\$3) same delay\$3 and with memory ((insert\$3 or add\$3) same delay\$3 and register) and cyclical\$3 with address\$3 with memory add (shift near4 register) and cyclical\$3 with address\$3 with memory add<20000920	.2:47
register) same cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) same (shift near4 register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory 40 ((insert\$3 or add\$3) same delay\$3 and with memory ((insert\$3 or add\$3) same delay\$3 and register) and cyclical\$3 with address\$3 with memory and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920	
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register) same cyclical\$3 with address\$3 with memory) and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 USPAT; EPO; JPO EPO; JPO	2:49
with memory) and @ad<20000920 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 USPAT; EPO; JPO EPO; JPO	2:49
16 40 (insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 USPAT; EPO; JPO	2:49
(memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 EPO; JPO USPAT; EPO; JPO	
register) and cyclical\$3 with address\$3 with memory ((insert\$3 or add\$3) same delay\$3 and (memory or buffer\$3) and (shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 register) and cyclical\$3 with address\$3	_,,,
17 40 ((insert\$3 or add\$3) same delay\$3 and (Shift near4 register) and cyclical\$3 with address\$3 with memory) and @ad<20000920 USPAT; EPO; JPO	
(memory or buffer\$3) and (shift near4 EPO; JPO register) and cyclical\$3 with address\$3 with memory) and @ad<20000920	i
register) and cyclical\$3 with address\$3 with memory) and @ad<20000920	2:52
with memory) and @ad<20000920	
18 32 (((insert\$3 or add\$3) same delay\$3 and USPAT: 2003/09/29 1	0 40
2000/03/23 2	2:49
(memory or buffer\$3) and (shift near4 EPO; JPO register) and cyclical\$3 with address\$3	
with memory) and @ad<20000920) and ((base	
near4 station) or MS)	
20 1 (insert\$3 or add\$3) same delay\$3 and (base USPAT; 2003/09/29 1	2:50
with station) and (shift near4 register) EPO; JPO	
and cyclical\$3 with address\$3 with memory	i
22 56 (base near4 station) same (memory or USPAT; 2003/09/29 1	2:52
buffer\$3) same shift with register EPO; JPO	
1 ((base near4 station) same (memory or USPAT; 2003/09/29 1	2:52
buffer\$3) same shift with register) and EPO; JPO	ļ
cyclical\$3 with address\$3 with memory 613 (base near4 station) and (memory or USPAT; 2003/09/29 1	3.00
24 613 (base near4 station) and (memory or USPAT; 2003/09/29 1 buffer\$3) same shift with register EPO; JPO	3:00
25 7 ((base near4 station) and (memory or USPAT; 2003/09/29 1	2:57
buffer\$3) same shift with register) and EPO; JPO	,
cyclical\$3 with address\$3 with memory	
26 6 (((base near4 station) and (memory or USPAT; 2003/09/29 1	2:59
buffer\$3) same shift with register) and EPO; JPO	
cyclical\$3 with address\$3 with memory) and	
@ad<20000920	
6 ((((base near4 station) and (memory or USPAT; 2003/09/29 1	2:54
buffer\$3) same shift with register) and EPO; JPO	
cyclical\$3 with address\$3 with memory) and @ad<20000920) and delay\$3	
	3.01
28 10 ((base near4 station) and (memory or USPAT; 2003/09/29 1. buffer\$3) same shift with register) and EPO; JPO	2:01
cyclical\$3 with address\$3	İ
9 (((base near4 station) and (memory or USPAT; 2003/09/29 1	3:00
buffer\$3) same shift with register) and EPO; JPO	
cyclical\$3 with address\$3) and	
@ad<20000920	
31 56 (base near4 station) same (memory or USPAT; 2003/09/29 13	3:00
buffer\$3) same shift with register EPO; JPO	

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C:\APPS\EAST\Workspaces\Default EAST Workspace (Flat Panel LANDSCAPE).wsp

32	54	((base near4 station) same (memory or	USPAT;	2003/09/29 13:00
		buffer\$3) same shift with register) and	EPO; JPO	
		@ad<20000920		
34	3	(((base near4 station) same (memory or	USPAT;	2003/09/29 13:03
	ŀ	buffer\$3) same shift with register) and	EPO; JPO	
		@ad<20000920) and cyclical\$3		
35	2	((((base near4 station) same (memory or	USPAT;	2003/09/29 13:03
		buffer\$3) same shift with register) and	EPO; JPO	
	l	@ad<20000920) and cyclical\$3) and delay\$3	1	